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SUPPLEMENTARY INFORMATION

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Phonon black-body radiation limit for heat dissipation in electronics

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S1: Additional information on MMIC

We show photographs of the inside and outside of the 4-16 GHz MMIC LNA chassis including the matching network in Figure 1. When aiming for lowest noise performance, the matching network and performance of the first stage ultimately sets the noise performance. To avoid substrate losses, and consequently degraded noise performance, an external input matching network on a low loss substrate was used. To decrease the magnitude of S_{11} (input reflection coefficient) and improve stability, a high inductance source microstrip was used on the first transistor.

To achieve flat in-band noise, an impedance matching tradeoff has to be done. The minimum noise temperature of an InP HEMT varies nearly linearly with frequency [1]. Therefore, the best approach to obtain a flat noise temperature within a certain frequency band is by noise matching the first stage at the upper frequency limit, while allowing a certain mismatch at the lower frequencies. The second and third stages were matched for flat gain, stability and output match. The LNA has a common bias network for all three stages.

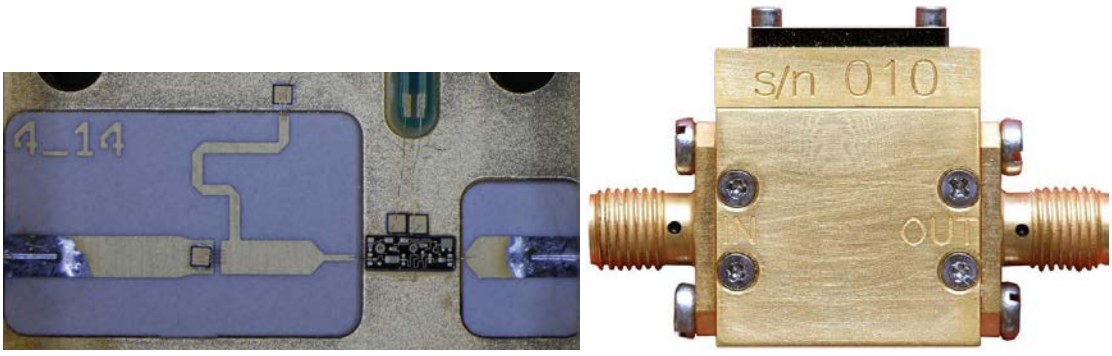

Fig. 1. Inside and outside of 4-16 GHz LNA chassis showing MMIC, input and output matching network, and stabilizing capacitors.

S2: Additional information on noise model and parameter extraction

The noise model and method used for noise parameter extraction is the same as in [2]. The principle of the model is that the noise in the device can be represented by thermal and non-thermal sources. Thermal noise is due to resistive elements in the amplifier, with the magnitude depending on the value of the resistances and the physical temperature. The only non-thermal noise source is hot-electron noise source in the output of the InP high electron mobility transistors (HEMTs). This noise source is typically modeled as an elevated drain temperature T_d that is a few orders of magnitude larger than the physical temperature of the HEMT. If the ambient temperature T_a of the LNA is known and the noise parameters are measured using the Agilent Noise Figure Analyzer, T_d can be obtained by fitting the simulated and

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measured noise temperatures of the LNA. We have previously shown that the circuit model accurately reproduces the noise characteristics of similar cryogenic amplifiers [2].

This procedure assumes that the LNA temperature equals the ambient temperature and results in a drain temperature that decreases linearly for T_a>40 K but appears to saturate at lower temperatures. This saturation is not easily explained using circuit theory. We therefore attribute the saturation to thermal noise and linearly extrapolate T_d for T_a<40 K. We then input this extrapolated T_d into the noise model to estimate the physical temperature required to explain the additional noise above the ideal prediction. This procedure is accomplished by varying the physical temperature of the noise sources inside the HEMT (including the output resistance and T_d) to match the simulated and measured noise temperatures. We employed this procedure to obtain the measured intrinsic temperature rises in Fig. 3b.

S3: Justification for adiabatic boundary condition under gate

We can estimate the heat leakage through the gate by modeling it as a fin with the ends connected the gate pads that act as thermal reservoirs. The fin length is equal to 100 microns, or the width of the gate in the direction perpendicular to the cross-section shown in the main text. Heat is generated by Joule heating uniformly under the gate in the perpendicular direction and then conducts into the gate. We assume that the temperature in the substrate under the gate is the peak temperature calculated using the phonon MC simulations. The temperature of the fin T(x) can then be written as:

$$\frac{T(x)-T_\infty}{T_b-T_\infty}=e^{-mx}$$

where T_b≈0 K is the ambient temperature, T_∞≈20 K is the temperature under the gate, and $m=\sqrt{(hP/kA_c)}$ is the fin parameter. Here h≈10 MW/m^{2}K is the substrate-gate interface conductance at an ambient temperature of 20 K, P=100 nm is the gate width, k=12 W/mK is the thermal conductivity of the gate, and A_c=0.15 μm^2 is the gate cross-sectional area. The thermal conductivity of the gate is obtained using the measured electrical resistivity of the gate and the Wiedemann-Franz law.

We estimate the length over which the temperature of the gate transitions from the ambient temperature to the peak temperature as L=1/m=1.35 microns, which is much smaller than the gate length of 100 microns. Therefore end effects can be safely neglected and the gate treated as isothermal with the substrate.

[1] J. Schleeh, G. Alestig, J. Halonen, A. Malmros, B. Nilsson, P. A. Nilsson, J. P. Starski, N. Wadefalk, H. Zirath, and J. Grahn, "Ultralow-power Cryogenic InP HEMT With Minimum Noise Temperature of 1 K at 6 GHz," *IEEE Electron Device Letters,* vol. 33, pp. 664-6, 2012.

[2] J. Schleeh, H. Rodilla, N. Wadefalk, P. A. Nilsson, and J. Grahn, "Characterization and Modeling of Cryogenic Ultra-Low Noise InP HEMT," *IEEE Transactions on Electron Devices,* vol. 60, pp. 206-212, 2013.